REMARKS

Claims 2-6 and 8-9 stand objected to because of noted informalities. Claims 4-6 stands rejected under 35 USC §102(b) as being anticipated by Chen, U.S. patent 6,078,195 and rejected under 35 USC §102(b) as being anticipated by Helm et al., U.S. patent 6,849,492. Claims 1-3 and 7-9 stands rejected under 35 USC §103(a) as being unpatentable over Jones et al., U.S. patent 5,666,288 in view of Chen, U.S. patent 6,078,195.

Claims 1-9 have been amended to more clearly state the invention and to correct the noted informalities with respect to claims 2-6 and 8-9. Reconsideration and allowance of each of the pending claims 1-9, as amended, is respectfully requested.

Chen, U.S. patent 6,078,195 discloses logic books with mixed low Vt and regular Vt devices provide a performance gain without the large increase in stand-by power of the logic book. Low Vt devices are used to gain speed, and regular Vt devices are used to cut off the off-current of the logic book. The optimization of mixed Vt configurations is important. No single path between an output and ground can be made of all low Vt devices, and no single path between the output and Vdd can be made of all low Vt devices. Generally, devices that are connected to Vdd and ground should be regular Vt devices, a low Vt devices should be connected closest to the output. All low Vt devices should be appropriately reversely biased in their off states. Because its merits in standby power, speed and noise margin, such mixed-low-and-regular-Vt logic books can have a wide use in VLSI designs (e.g., high performance microprocessor design).

Helm et al., U.S. patent 6,849,492 discloses wells that are formed in a substrate where standard Vt and low Vt devices of both a first and second type are to be fabricated. Wells defining the locations of first type standard Vt devices are masked, and a first voltage threshold implant adjustment is performed within wells defining the second type standard Vt devices, and each of the first and second type low Vt devices. Wells that define the locations of second type standard Vt devices are masked, and a second voltage threshold implant adjustment is performed to the wells defining the first type standard Vt devices, and each of the first and second type low Vt devices. Doped polysilicon gate stacks are then formed over the wells. Performance characteristics and control of each device Vt is controlled by regulating at least one of the first and second voltage threshold implant adjustments, and the polysilicon gate stack doping.

Jones et al., U.S. patent 5,666,288 discloses a method and apparatus for designing and manufacturing integrated circuits (ICs) that involves providing an initial library of IC cells (106) and a behavioral circuit model (100) in order to create a gate schematic netlist (102). The gate schematic netlist (102) is optimized by changing individual transistor sizes, power rail sizes, cell pitch, and the like in a step (103). Once the optimization has occurred, the initial library can no longer be used to place and route the IC. Therefore, a hybrid logic cell library is created from the gate schematic netlist (102) via a step (105). This hybrid library and the above optimizations provides a placed and routed IC via a step (126) in a short design cycle while optimizing performance of the IC.

In accordance with features of the present invention, all the PFETs in the

SVT circuit library are replaced with LVT PFETs. Due to the nature of PFETs, PFETs are larger and slower than NFETs in any given CMOS technology. Converting the SVT PFETs to LVT PFETs results in a much faster rise time for any given circuit. The SVT NFET controls the leakage current to ground when the NFET is in the off state. Assuming an even distribution of "1" and "0" states on a chip, the SVT NFET keeps the leakage current to one-half the leakage current that an equivalent LTV circuit would allow. The fall time of the SVT NFET remains the same, but the circuit is more balanced because the faster rise time of the LVT PFETs more closely matches the fall time of SVT NFET's.

As recited in independent claim 4, as amended, each said hybrid AVT circuit including a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs); each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

There are significant differences between what is disclosed in the Chen and Helm et al. patents and the pending claims 4-6, as amended; and the Examiner is respectfully requested to withdraw the rejections under 35 U.S.C. §102 because it is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention (Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379, 231 USPQ 81, 90 (Fed. Cir. 1986)).

Only Applicants teach an alternate voltage threshold (AVT) circuit library with each P-channel field effect transistor (PFET) having a low voltage threshold (LVT);

and each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT). Applicant respectfully submits the disclosures of the Chen and Helm et al. patents do not disclose, nor suggest the subject matter or limitations as expressly recited in independent claim 4, as amended. Chen and Helm et al. teach the use of PFETs and NFETs having both a low voltage threshold (LVT) and a standard voltage threshold (SVT). Thus, independent claim 4 is patentable.

Dependent claims 5-6 depend from patentable claim 4, further defining the invention. Each of the dependent claims 5-6, as amended, is likewise patentable. Reconsideration and allowance of each of the pending claims 4-6, as amended, is respectfully requested.

Independent claims 1 and 7 respectively recite a method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs and a computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system. Each of the independent claims 1 and 7, as amended, recites the steps of identifying standard voltage threshold (SVT) circuits in a circuit library; for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library.

Applicants respectfully submit that as amended, each of the independent

claims 1 and 7 more clearly states the invention and is patentable of all of the references of record including the Chen and Jones et al. patents.

The subject matter of the invention, as recited in each of the independent claims 1 and 7, is not rendered obvious from the total teaching of Chen and Jones et al. Only Applicants teach each of the steps: for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library. Applicant respectfully submits that the prior art description of Chen and Jones et al. falls short of applicant's invention, and the subject matter of the claimed invention as recited in claims 1 and 7, as amended, would not have been obvious to one of ordinary skill in the art in view of the references of record. Further in the cited references, there is no hint of for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library, as taught and claimed by Applicants. A combination of all the teachings of the references of record would not achieve the claimed invention as recited by claims 1 and 7, as amended. These steps are not suggested from the total teaching of Chen and Jones et al. The prior art of record, including Chen and Jones et al. provides no teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having

ordinary skill in the art to achieve the claimed invention. Thus, each of the independent claims 1 and 7, as amended, is patentable.

Dependent claims 2-3, and 8-9 respectively depend from patentable claims 1 and 7, further defining the invention. Each of the dependent claims 2-3, and 8-9, as amended, is likewise patentable. Reconsideration and allowance of each of the pending claims 2-3, and 8-9, as amended, is respectfully requested.

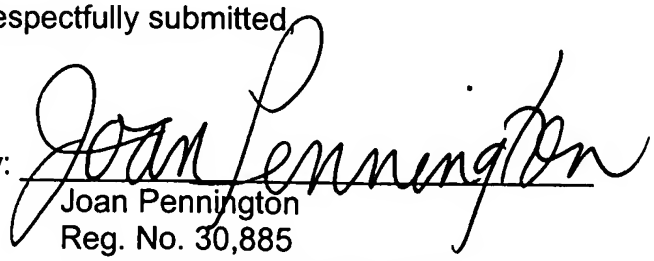
Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

Reconsideration and allowance of each of the pending claims 1-9, as amended, is respectfully requested.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-9, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: 

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